PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2002-074945

(43)Date of publication of application : 15.03.2002

(51)Int.Cl. G11C 11/406
G11C 11/407
G11C 11/403

(21)Application number : 2000-265053

(22)Date of filing : 01.09.2000

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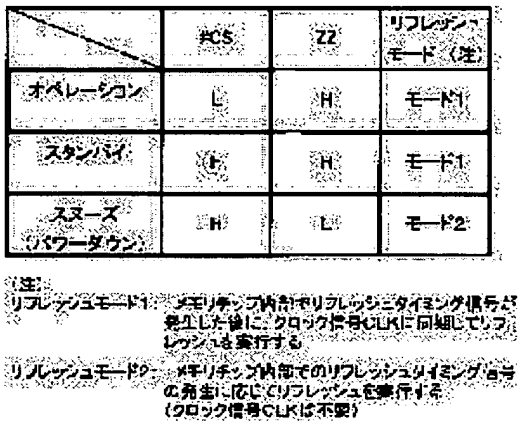
(54) REFRESH CONTROL OF SEMICONDUCTOR MEMORY

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a technique through which refresh operations suitable to a plurality of respective operating states that a semiconductor memory can take are performed.

SOLUTION: A memory chip 200 starts a refresh operation in synchronism with a clock signal CLK supplied from an external device in an operation cycle after the generation of a refresh timing signal RFTM. Moreover, in a snooze state (a low power consumption state), a refresh operation is started in accordance with the generation of the signals RFTM regardless of the presence or absence of the signal.



	/CS	ZZ	リフレッシュモード（注）
オペレーション	L	H	モード1
スタンバイ	H	H	モード1
スヌーズ（パワーダウン）	H	L	モード2

（注）
リフレッシュモード1：メモリチップ内部でリフレッシュタイミング信号が発生した後に、クロック信号CLKに同期してリフレッシュを実行する
リフレッシュモード2：メモリチップ内部でのリフレッシュタイミング信号の発生に応じてリフレッシュを実行する（クロック信号CLKは不要）

LEGAL STATUS

[Date of request for examination] 07.09.2001

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] A memory cell array which is semiconductor memory equipment and has a dynamic mold memory cell, It has a refresh timer which generates a refresh timing signal used for decision of activation timing of refresh actuation of said memory cell array. A refresh control section which makes said memory cell array perform refresh actuation, corresponding at least to said refresh timing signal, An operating state signal input terminal for receiving an operating state signal which specifies operating state of said semiconductor memory equipment from an external device, An external timing signal input terminal for receiving an external timing signal used with said refresh timing signal in case said refresh control section determines activation timing of said refresh actuation from an external device, When the (i) aforementioned operating state signal shows the 1st operating state, a preparation and said refresh control section Internal refresh is performed according to the 1st refresh mode which makes said memory cell array start refresh actuation after generating of said refresh timing signal according to timing determined by said external timing signal. (ii) when said operating state signal shows the 2nd operating state Semiconductor memory equipment characterized by performing internal refresh according to the 2nd refresh mode which makes said memory cell array start refresh actuation irrespective of existence of said external timing signal according to generating of said refresh timing signal.
[Claim 2] It is semiconductor memory equipment which is semiconductor memory equipment according to claim 1, and includes a low-power condition with less power consumption than said 1st operating state impossible [read-out and writing of data in said semiconductor memory equipment] including a read/write cycle in which said 1st operating state has possible at least read-out of data in said semiconductor memory equipment and one side of writing as for said 2nd operating state.
[Claim 3] It is semiconductor memory equipment with which are semiconductor memory equipment according to claim 1 or 2, said external timing signal is a clock signal, and said refresh control section makes said memory cell array perform refresh actuation after generating of said refresh timing signal in said 1st refresh mode synchronizing with said clock signal by said semiconductor memory equipment performing a read/write cycle in said 1st operating state synchronizing with said clock signal.
[Claim 4] It is semiconductor memory equipment according to claim 3, and has the clock control section for controlling further said clock signal supplied from said external device. Said clock control section When said semiconductor memory equipment is in said 1st operating state Semiconductor memory equipment which suspends supply of said clock signal in said specific circuit when said semiconductor memory equipment is in said 2nd operating state, while supplying said clock signal to a specific circuit containing said refresh control section in said semiconductor memory equipment.
[Claim 5] Said 2nd operating state is semiconductor memory equipment whose power consumption of said semiconductor memory equipment it is semiconductor memory equipment according to claim 4, and is in lowest condition.
[Claim 6] It is semiconductor memory equipment according to claim 1 to 5, and said memory cell array is divided into two or more blocks. Said refresh control section In the case of initiation of refresh actuation by said 1st refresh mode When read-out or writing of data is performed in one block in a block of said plurality While performing refresh actuation in blocks other than a block with which read-out or writing of said data is performed Semiconductor memory equipment which makes the block concerned perform refresh actuation after said read-out or writing is completed about a block with which read-out or writing of said data is performed.
[Claim 7] A memory cell array which has a dynamic mold memory cell A refresh timer which generates a refresh timing signal used for decision of activation timing of refresh actuation of said memory cell array When it is the refresh control method equipped with the above, it is the method of controlling refresh of said memory cell array and the (i) aforementioned semiconductor memory equipment is in the 1st operating state Internal refresh is performed according

to the 1st refresh mode in which said memory cell array starts refresh actuation according to timing determined by predetermined external timing signal given from an external device after generating of said refresh timing signal. (ii) when said semiconductor memory equipment is in the 2nd operating state Irrespective of existence of said external timing signal, it is characterized by performing internal refresh according to the 2nd refresh mode in which said memory cell array starts refresh actuation according to generating of said refresh timing signal.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] This invention relates to refresh control of semiconductor memory equipment.
[0002]
[Description of the Prior Art] DRAM and SRAM are used as semiconductor memory equipment. DRAM is cheap compared with SRAM, and although it is large capacity, refresh actuation is required as known well. On the other hand, although SRAM of refresh actuation is unnecessary and it is easy to use, compared with DRAM, it is expensive, and capacity is small.
[0003] It considers as semiconductor memory equipment equipped with both of advantages of DRAM and SRAM, and false [SRAM] (referred to as VSRAM or PSRAM) is known. False [SRAM] builds in the refresh control section and is performing refresh actuation inside while it is equipped with the memory cell array which consisted of same dynamic mold memory cells as DRAM. For this reason, the external device (for example, CPU) connected to false [SRAM] can access false [SRAM], without being conscious of refresh actuation (read-out and writing of data). Such a feature false [SRAM] is called "permeability of refresh."
[0004]
[Problem(s) to be Solved by the Invention] By the way, there are false [SRAM / which can take two or more operating state / some] like for example, a normal operation condition or a power-saving condition. In such false [SRAM], sufficient consideration was not made about how internal refresh should be performed in each operating state. Such a problem is a problem common to the semiconductor memory equipment of the dynamic mold which contained not only false [so-called / SRAM] but the refresh timer, and the refresh control section.
[0005] This invention is made in order to solve the conventional technical problem mentioned above, and it aims at offering the technology in which refresh actuation which was suitable for two or more operating state which semiconductor memory equipment can take, respectively can be performed.
[0006]
[The means for solving a technical problem, and its operation and effect] In order to attain the above-mentioned purpose, the semiconductor memory equipment by this invention It has the refresh timer which generates the refresh timing signal used for the decision of the activation timing of refresh actuation of the memory cell array which has a dynamic mold memory cell, and said memory cell array. The refresh control section which makes said memory cell array perform refresh actuation, corresponding at least to said refresh timing signal, The operating state signal input terminal for receiving the operating state signal which specifies the operating state of said semiconductor memory equipment from an external device, It has the external timing signal input terminal for receiving the external timing signal used with said refresh timing signal in case said refresh control section determines the activation timing of said refresh actuation from an external device. moreover, when the (i) aforementioned operating state signal shows the 1st operating state, said refresh control section Internal refresh is performed according to the 1st refresh mode which makes said memory cell array start refresh actuation after generating of said refresh timing signal according to the timing determined by said external timing signal. (ii) when said operating state signal shows the 2nd operating state Irrespective of the existence of said external timing signal, internal refresh is performed according to the 2nd refresh mode which makes said memory cell array start refresh actuation according to generating of said refresh timing signal.
[0007] In the 1st operating state of the above, since internal refresh is started according to the timing determined by the external timing signal, a refresh control section can perform easily mediation with access from an external device, and internal refresh. It is possible to perform internal refresh on the other hand, also when an external timing signal is not

inputted, for example since internal refresh is started irrespective of the existence of an external timing signal in the 2nd operating state according to generating of a refresh timing signal. That is, it is possible to perform refresh actuation which was suitable for two or more operating state, respectively with the above-mentioned semiconductor memory equipment.
[0008] In addition, you may make it said 1st operating state contain the read/write cycle in which at least read-out of the data in said semiconductor memory equipment and one side of writing are possible. Moreover, you may make it said 2nd operating state include a low-power condition with less power consumption than said 1st operating state impossible [read-out and the writing of data in said semiconductor memory equipment].
[0009] In this gestalt, also when internal refresh can be performed and there is no input of the signal from the outside in the state of a low power, performing read-out of data and mediation with writing and internal refresh in a read/write cycle, it is possible to perform internal refresh actuation.
[0010] Said external timing signal is a clock signal, and said semiconductor memory equipment may be made to perform a read/write cycle in said 1st operating state synchronizing with said clock signal. Moreover, as for said refresh control section, in said 1st refresh mode, it is desirable to make said memory cell array start refresh actuation after generating of said refresh timing signal synchronizing with said clock signal.
[0011] With this gestalt, since a read/write cycle and internal refresh are performed by each synchronizing with a clock signal, there is an advantage of being easy to arbitrate both.
[0012] As for said semiconductor memory equipment, it is desirable to have the clock control section for controlling further said clock signal supplied from said external device. When said semiconductor memory equipment is in said 1st operating state, while this clock control section supplies said clock signal to the specific circuit containing said refresh control section in said semiconductor memory equipment, when said semiconductor memory equipment is in said 2nd operating state, it may suspend supply of said clock signal in said specific circuit.
[0013] It is possible to reduce the power consumption of semiconductor memory equipment more in the 2nd operating state with this gestalt.
[0014] In addition, said 2nd operating state is good though the power consumption of said semiconductor memory equipment is in the lowest condition.
[0015] Power consumption is able to ensure internal refresh also in the lowest operating state with this gestalt.
[0016] Said memory cell array is divided into two or more blocks. In addition, said refresh control section In the case of initiation of the refresh actuation by said 1st refresh mode When read-out or the writing of data is performed in one block in the block of said plurality While performing refresh actuation in blocks other than the block with which read-out or the writing of said data is performed After said read-out or writing is completed about the block with which read-out or the writing of said data is performed, it is desirable that it is the thing which makes the block concerned perform refresh actuation.
[0017] also when the data from an external device carries out reading appearance temporarily or the demand of writing and the timing of internal refresh occur in coincidence with this gestalt, performing immediately is possible, without delaying read-out and the writing of data. Therefore, it is possible to secure the so-called permeability of refresh.
[0018] In addition, this invention can be realized with various gestalten, for example, can be realized with gestalten, such as the control method of semiconductor memory equipment, its refresh control method, the semiconductor memory system equipped with semiconductor memory equipment and a control unit, and semiconductor memory equipment, and electronic equipment equipped with semiconductor memory equipment.
[0019]
[Embodiment of the Invention] Next, the gestalt of operation of this invention is explained in order of the following based on an example.
A. Example of application:D. modification to the refresh actuation:B. 2nd example:C. electronic equipment of 1st example:, A1, the terminal configuration of a memory chip, the internal configuration of whole outline:-A2. circuit configuration: and A3. refresh control section of operating state, and the whole whole : of operation and A4. chip :
[0020] A. 1st example: -- the terminal configuration of an A1. memory chip, and outline [of operating state]: -- drawing 1 is explanatory drawing showing the configuration of the terminal of the memory chip 200 as the 1st example of this invention. The memory chip 200 has the following terminals.
[0021] CLK: A clock input terminal, A0 - an A19:address input terminal (20), a #CS:chip-select input terminal, ZZ:SUNUZU input terminal, a #WE:write-enable input terminal, a #OE:output-enable input terminal, a #LB:lower-byte enabling input terminal, a #UB:high-order-byte enabling input terminal, IO0-IO15: I / O data terminal (16).
[0022] In addition, in the following explanation, the same sign as a terminal name and a signal name is used. That by which "#" is given to the head of a terminal name (signal name) means that it is negative logic. Although the address

input terminals A0-A19 and two or more I / O data terminals IO0-IO15 are formed, respectively, by drawing 1 , it is simplified and they are drawn.
[0023] This memory chip 200 is constituted as false [which can be accessed in the almost same procedure as SRAM / SRAM] (VSRAM). The refresh control section containing the refresh timer 70 is built in the memory chip 200. refresh actuation according read-out of the data from an external device (it is also called a "memory control unit" or a "control unit"), and actuation of writing to "external access", a call, and the built-in refresh control section with this specification -- "internal refresh" -- or it is only called "refresh."
[0024] A clock signal CLK is used as a synchronizing signal for taking the synchronization with initiation of external access, and initiation of internal refresh. That is, the addresses A0-A19 and chip select signal #CS are inputted from an external device synchronizing with a clock signal CLK. Moreover, internal refresh is also usually performed synchronizing with this clock signal CLK. The built-in refresh control section is performing mediation with external access and internal refresh synchronizing with this clock signal CLK.
[0025] In addition, in this specification, the signal does not necessarily mean generating at the same time of day as the edge of a clock signal CLK, and **** "a certain signal synchronizes with a clock signal CLK" means maintaining the edge of a clock signal CLK, and fixed time relation, and generating.
[0026] Chip select signal #CS and the SUNUZU signal ZZ are signals for controlling the operating state of a memory chip 200. Drawing 2 is explanatory drawing showing the partition of the operating state of the memory chip 200 according to the signal level of chip select signal #CS and the SUNUZU signal ZZ. In addition, in this specification, "H level" means "1" level of the two level of a binary signal, and "L level" means "0" level.
[0027] When chip select signal #CS is [the SUNUZU signal ZZ] H level on L level (active), a read/write operation cycle (it is only hereafter called an "operation cycle" or a "read/write cycle") is performed. In an operation cycle, read-out and the writing of the data in a memory chip 200 are performed.
[0028] A standby cycle is performed when both chip select signal #CS and the SUNUZU signal ZZ are H level. Let all word lines be non-active states in a standby cycle. However, when internal refresh is performed, the word line specified by the refresh address is activated.
[0029] If the SUNUZU signal ZZ is set to L level when chip select signal #CS is H level (inactive), a memory chip 200 will shift to a SUNUZU condition (it is also called a "powered down state"). In the SUNUZU condition, it has stopped except a circuit required for refresh actuation. Moreover, in the state of SUNUZU, it is stopped by the clock signal CLK in the memory chip 200 interior. Since there is very little power consumption in the state of SUNUZU, it is suitable for backup of the data in memory.
[0030] By the operation cycle and the standby cycle, refresh actuation is performed according to the 1st refresh mode, and is performed according to the 2nd refresh mode in the SUNUZU condition. In the 1st refresh mode, after the refresh timer 70 generates a refresh timing signal, refresh actuation is started synchronizing with a clock signal CLK. On the other hand, in the 2nd refresh mode, shortly after the refresh timer 70 generates a refresh timing signal, refresh actuation is started. Since refresh actuation with the 2nd refresh mode is performed to a clock signal CLK and asynchronous, the clock signal CLK is unnecessary. Thus, this memory chip 200 performs refresh according to the refresh mode which was suitable for three operating state, respectively. About the details of the refresh actuation in these two modes, it mentions later.
[0031] Chip select signal #CS and the SUNUZU signal ZZ are equivalent to "the operating state signal which specifies the operating state of semiconductor memory equipment" in this invention so that he can understand from above-mentioned explanation. Moreover, a clock signal CLK is equivalent to "the external timing signal used with a refresh timing signal in case the activation timing of refresh actuation is determined" in this invention.
[0032] Signals other than three signals CLK and #CS which mentioned above, and ZZ are almost the same as what is used for the usual memory chip. The addresses A0-A19 are 20 bits, and specify the address of 1 mega word. Moreover, I / O datas IO0-IO15 are 16-bit data for 1 word. That is, one value of the addresses A0-A19 supports 16 bits (1 word), and 16-bit I / O datas IO0-IO16 can be outputted and inputted at once.
[0033] In an operation cycle, if write enable signal #WE is set to L level, a light cycle will be performed, and if set to H level, a read cycle will be performed. Moreover, if output enable signal #OE is set to L level, the output from input/output terminals IO0-IO15 will be attained. Lower byte enable signal #LB and high-order byte enabling input signal #UB are the control signals for performing read-out and writing only about any 1 byte in the lower byte of 1 word (16 bits), and a high-order byte. For example, if lower byte enable signal #LB is set as L level and high-order byte enable signal #UB is set as H level, read-out and writing will be performed only about 8 bits of 1-word low order. In addition, the power supply terminal is omitted in drawing 1 .
[0034] Drawing 3 is a timing chart which shows the outline of actuation of the memory chip 200 of the 1st example. It

is judged synchronizing with the rising edge of a clock signal CLK any of three operating state (operation, standby, SUNUZU) shown in drawing 2 they are. The first three cycles of drawing 3 are operation cycles. an operation cycle -- the level of write enable signal #WE -- responding -- reading appearance -- carrying out (read cycle) -- either which is written in (light cycle) is performed. In addition, the 1 period Tc of a clock signal CLK is the same as the cycle time (it is also called a "cycle period") of this memory chip 200. Clock period Tc is set as the value of the range for about 50 to about 100ns.

[0035] In the 4th cycle of drawing 3 , since chip select signal #CS has started on H level, a standby cycle is started. In the 5th cycle, further, since the SUNUZU signal ZZ has fallen on L level, a memory chip 200 will be in a SUNUZU condition.

[0036] In addition, chip select signal #CS and the addresses A0-A19 are inputted from an external device (for example, CPU) in the signal shown in drawing 3 synchronizing with a clock signal CLK. Specifically, as for chip select signal #CS and the addresses A0-A19, only predetermined time amount (setup time) is early inputted into a memory chip 200 rather than the rising edge of a clock signal CLK. This reason is for making it these signal #CS and the value of A0-A19 decided in the rising edge of a clock signal CLK.

[0037] The whole A2. circuit configuration: Drawing 4 is the block diagram showing the internal configuration of a memory chip 200. This memory chip 200 is equipped with the data input output buffer 10, the memory cell array 20, and the address buffer 60. The memory cell array 20 is divided into four blocks 20A-20D. 1st block 20A has memory cell subarray 22A, line decoder 24A, and train decoder 26A. Other blocks 20B-20D are the same. Since the configuration of Blocks 20A-20D is identitas, below, 1st block 20A and other circuits relevant to this are mainly explained.

[0038] One configuration of block 20A is the same as the memory cell array of typical DRAM. Namely, as for subarray 22A, two or more memory cells of a 1 transistor 1 capacitor mold are arranged in the shape of a matrix. The word line and the bit line pair are connected to each memory cell. Moreover, a precharge circuit, a sense amplifier, etc. which are not illustrated are formed in subarray 22A. Line decoder 24A chooses one in two or more word lines in subarray 22A, and is activated. Train decoder 26A chooses the bit line pair for 1 word (16 bits) in two or more sets of bit line pairs in subarray 22A as coincidence. Therefore, an external device can access the 16 bits (1 word) data within one block by inputting the one addresses A0-A19 at coincidence.

[0039] The 20-bit addresses A0-A19 are inputted into the address buffer 60 shown in the lower left side of drawing 4 . The addresses A0-A19 are latched within an address buffer 60 synchronizing with a clock signal CLK, and are supplied to other circuits. The 2-bit lowest addresses A0-A1 are used as a block address for choosing any one of four blocks 20A-20D. Moreover, the 6-bit addresses A2-A7 of a high order are used by block addresses A0-A1 as the train address, and other 12-bit addresses A8-A19 are used as a line address rather than them. Therefore, one of four blocks 20A-20D is chosen by block addresses A0-A1, and the data for 1 word (16 bits) is chosen by the train addresses A2-A7 and line addresses A8-A19 from the selected blocks. Through the data input output buffer 10, reading appearance of the data for selected 1 word is carried out, or it is written in.

[0040] Line PURIDE coder 30A, block controller 40A, and refresh demand signal generating circuit 50A are connected to one block 20A at this order. It is the same about other blocks 20B-20D. In the memory chip 200, the refresh timer 70, the clock controller 80, the refresh counter controller 90, and the refresh counter 100 are formed further.

[0041] The refresh timer 70 is a circuit which generates refresh timing signal RFTM for every fixed refresh period. The refresh timer 70 is constituted by for example, the ring oscillator. The refresh period is set as about 32 microseconds.

[0042] When the SUNUZU signal ZZ is H level, the clock controller 80 generates the internal clock signal ICLK from the clock signal CLK inputted from the external device, and supplies it to other circuits in a memory chip 200. The internal clock signal ICLK has the same period as the external clock signal CLK, and is a signal with smaller duty. For example, the duty of the internal clock signal ICLK is about 3% to the duty of the external clock signal CLK being about 50%. Therefore, in the following explanation, the explanation of "synchronizing with the internal clock signal ICLK" means synchronizing also with the external clock signal CLK. In addition, the small internal clock signal ICLK of duty is created for making the synchronization with a clock signal easy to take in the interior of a memory chip 200. In addition, it is also possible to use the external clock signal CLK as it is, without creating the internal clock signal ICLK.

[0043] When the SUNUZU signal ZZ is L level, the clock controller 80 suspends supply of the internal clock signal ICLK. That is, even if the external clock signal CLK is inputted in the state of SUNUZU, supply of the internal clock signal ICLK in other circuits of the memory chip 200 interior will be suspended. Consequently, in the state of SUNUZU, since actuation is suspended, circuits other than the circuit which performs internal refresh can stop power consumption very low. In addition, below, the internal clock signal ICLK is only called "clock signal ICLK."

[0044] The refresh demand signal generating circuits 50A-50D generate the refresh demand signals RFREQ0-RFREQ3 for each blocks 20A-20D according to refresh timing signal RFTM supplied from the refresh timer 70. These refresh demand signals RFREQ0-RFREQ3 are given to the corresponding block controllers 40A-40D, respectively.
[0045] The block addresses A0-A1 given from the external device with the refresh demand signals RFREQ0-RFREQ3 are supplied to the block controllers 40A-40D. The refresh demand signals RFREQ0-RFREQ3 mean what refresh actuation should be started for in four blocks 20A-20D. Moreover, by the operation cycle, block addresses A0-A1 show of any of four blocks 20A-20D external access is demanded. Then, the block controllers 40A-40D arbitrate external access and internal refresh to four blocks according to these signals RFREQ0-RFREQ3, and A0-A1. Specifically, this mediation is performed by setting up the level of external access implementation signal #EX0-#EX3, refresh implementation signal #RF0 - #RF3, respectively.
[0046] The line PURIDE coders 30A-30D choose one of the line addresses A8-A19 inputted from the external device, and the refresh addresses RFA8-RFA19 given from the refresh counter 100 according to the level of external access implementation signal #EX0-#EX3, refresh implementation signal #RF0 - #RF3, and supply it to the line decoders 24A-24D. Selection of this address is independently performed for every line PURIDE coder. for example, when there is a demand of refresh and the demand of external access to 1st block 20A is made by this and coincidence 1st line PURIDE coater 30A chooses line addresses A8-A19, and supplies them to 1st block 20A, and, on the other hand, other line PURIDE coaters 30B-30D supply refresh addresses RFA8-RFA19 to the blocks 20B-20D which choose and correspond, respectively.
[0047] In addition, about the refresh demand signal generating circuits 50A-50D, the block controllers 40A-40D, the configuration of the line PURIDE coders 30A-30D, and actuation, it mentions later further.
[0048] The refresh counter controller 90 detects whether the refresh actuation to the same refresh address was completed in all four blocks 20A-20D. This detection is performed by investigating level change of four refresh demand signals RFREQ0-RFREQ3 so that it may mention later. If the refresh actuation in four blocks 20A-20D is completed, the refresh counter controller 90 will supply count-up signal #CNTUP to the refresh counter 100. The refresh counter 100 counts up one value of refresh addresses RFA8-RFA19 according to this count-up signal #CNTUP.
[0049] Although the memory chip 200 has the controller which controls the operating state of the circuit in a chip outside the circuit shown in drawing 4 according to chip select signal #CS or the SUNUZU signal ZZ, the controller which controls an I/O condition according to various kinds of enable signal #WE(s), #OE, #LB, and #UB, it is omitted on [of illustration] expedient by drawing 4 .
[0050] In addition, the circuit portion constituted among the circuits shown in drawing 4 in the memory cell array 20, the data input output buffer 10, an address buffer 60, and circuits other than clock controller 80 (70 30A-30D, 40A-40D, 50A-50D, 90,100) is equivalent to the "refresh control section" in this invention. Moreover, especially the circuit portion that consists of line PURIDE coders 30A-30D, block controllers 40A-40D, and refresh demand signal generating circuits 50A-50D has the function as a mediation circuit to perform mediation with internal refresh and external access.
[0051] The internal configuration of A3. refresh control section, and actuation: Drawing 5 is the block diagram showing the internal configuration of refresh demand signal generating circuit 50A and block controller 40A. In addition, it has the configuration as these with other same refresh demand signal generating circuits 50B-50D and other block controllers 40B-40D.
[0052] Refresh demand signal generating circuit 50A is equipped with an inverter 52, NAND gate 54, a pulse generating circuit 55, two latch circuits 56 and 58, and AND gates 57.
[0053] The SUNUZU signal ZZ is inputted into one input terminal of NAND gate 54, and clock signal ICLK is reversed and inputted into the input terminal of another side with the inverter 52. The output Q54 of NAND gate 54 is inputted into the AND gate 57.
[0054] A pulse generating circuit 55 generates a pulse signal Q55 according to the rising edge of refresh timing signal RFTM. This pulse generating circuit 55 consists of one-shot multivibrators. The pulse signal Q55 is given to the 1st latch's 56 set input terminal. This latch's 56 output Q56 is inputted into the AND gate 57 with the output Q54 of NAND gate 54. The output Q57 of the AND gate 57 is supplied to the 2nd latch's 58 set input terminal. This latch's 58 output Q58 is supplied to block controller 40A as a refresh demand signal RFREQ0, and is inputted also into the 1st latch's 56 reset input terminal.
[0055] Block controller 40A is equipped with the external access implementation signal generating circuit 42, the refresh implementation signal generating circuit 44, and the pulse generating circuit 46. Chip select signal #CS, block addresses A0-A1, and clock signal ICLK are inputted into the external access implementation signal generating circuit 42. The refresh demand signal RFREQ0 is also inputted into the refresh implementation signal generating circuit 44

besides these signal #CS, A0-A1, and ICLK.
[0056] The external access implementation signal generating circuit 42 judges whether external access is demanded from block 20A relevant to this block controller 40A in the rising edge of clock signal ICLK. This judgment is made based on chip select signal #CS and block addresses A0-A1. That is, chip select signal #CS is L level (active), and when block addresses A0-A1 are "00", it is judged as what external access is demanded as from block 20A. At this time, the external access implementation signal generating circuit 42 sets external access implementation signal #EX0 as L level (active). moreover -- the time of there being no demand of external access to block 20A -- the external access implementation signal generating circuit 42 -- external access implementation signal #EX0 -- being inactive (H level) -- it sets up.
[0057] The refresh implementation signal generating circuit 44 as well as the external access implementation signal generating circuit 42 judges whether external access to block 20A is demanded. When there is no demand of external access to block 20A and there is a refresh demand, the refresh implementation signal generating circuit 44 sets refresh implementation signal #RF0 as L level (active). Moreover, when there is also no external access and refresh demand, refresh implementation signal #RF0 is set as H level (inactive). In addition, if refresh implementation signal #RF0 becomes active, the refresh actuation in block 20A will be started.
[0058] When there is a demand of external access to block 20A, even if there is a refresh demand, refresh implementation signal #RF0 is set as H level (inactive). Then, refresh implementation signal #RF0 is set as L level (active), after being held at H level and completing external access until external access to block 20A is completed. In addition, when external access to block 20A is completed, the case where it is the 1st as which external access to the block of those other than this block 20A is required [******], and the 2nd case where chip select signal #CS is set to H level (inactive), and serves as a standby cycle exist. The refresh implementation signal generating circuit 44 investigates whether whenever the rising edge of clock signal ICLK occurred, either in [these] two occurred, and when either occurs, it sets refresh implementation signal #RF0 as L level (active). In this way, if refresh implementation signal #RF0 becomes active, the refresh actuation in block 20A will be started from the time.
[0059] A pulse generating circuit 46 generates short pulse-like reset-signal RESET0 according to the rising edge of refresh implementation signal #RF0. This pulse generating circuit 46 consists of one-shot multivibrators. This reset-signal RESET0 is given to the 2nd latch's 58 reset input terminal.
[0060] Drawing 6 is a timing chart which shows initiation of the refresh actuation in a standby cycle. In a standby cycle, since the SUNUZU signal ZZ (drawing 6 (c)) is H level, clock signal ICLK passes through NAND gate 54, and is inputted into the AND gate 57 (drawing 6 (e)).
[0061] At time of day t1, refresh timing signal RFTM (drawing 6 (f)) supplied from the refresh timer 70 starts on H level, and what refresh actuation should be started for by this is notified to refresh demand signal generating circuit 50A. If refresh timing signal RFTM starts on H level in time of day t1, a pulse signal Q55 (drawing 6 (g)) will occur, and the 1st latch's 56 output Q56 (drawing 6 (h)) will also start on H level according to this.
[0062] In the time of day t2 of the next rising edge of clock signal ICLK, the 1st latch's 56 output Q56 (drawing 6 (h)) is maintained at H level. Therefore, the output Q57 (drawing 6 (i)) of the AND gate 57 starts on H level according to change of the output Q54 of NAND gate 54, and sets the 2nd latch 58. Consequently, the refresh demand signal RFREQ0 (drawing 6 (j)) which is the 2nd latch's 58 output starts on H level.
[0063] In addition, at time of day t2, since chip select signal #CS and the SUNUZU signal ZZ all have H level, a standby cycle is performed after time of day t2, and external access is not performed. Therefore, the external access implementation signal generating circuit 42 holds external access implementation signal #EX0 (drawing 6 (k)) on H level (inactive).
[0064] The refresh implementation signal generating circuit 44 sets refresh implementation signal #RF0 (drawing 6 (l)) as L level (active) according to the refresh demand signal RFREQ0. Then, if sufficient time amount passes in order to perform refresh actuation, the refresh implementation signal generating circuit 44 will start refresh implementation signal #RF0 on H level (inactive). A pulse generating circuit 46 generates the pulse of reset-signal RESET0 according to the rising edge of refresh implementation signal #RF0 (drawing 6 (m)). Since this reset-signal RESET0 is given to the 2nd latch's 58 reset input terminal, the refresh demand signal RFREQ0 returns to L level (inactive) according to the pulse of reset-signal RESET0.
[0065] In addition, since the refresh demand signal RFREQ0 is inputted also into the 1st latch's 56 reset input terminal, this latch 56 is reset according to the standup of the refresh demand signal RFREQ0 (drawing 6 (h)). Consequently, clock signal ICLK is prevented by the AND gate 57, and the output Q57 of the AND gate 57 falls to L level.
[0066] In addition, it is started after the rising edge of clock signal ICLK in time of day t2, and one refresh actuation is completed in the 1 period Tc of clock signal ICLK (namely, cycle period of memory). Therefore, even if refresh

actuation is performed in the standby cycle, when external access is required in the next rising edge of clock signal ICLK, it is possible to carry out the external access immediately.
[0067] Drawing 7 is a timing chart which shows initiation of the refresh actuation in an operation cycle. If refresh timing signal RFTM (drawing 7 (f)) starts on H level in time of day t11, in the time of day t12 of the rising edge of the next clock signal ICLK, the refresh demand signal RFREQ0 (drawing 7 (j)) will start on H level. The actuation so far is the same as the actuation in the standby cycle shown in drawing 6 .
[0068] In the example of drawing 7 , since chip select signal #CS has fallen on L level in time of day t12, an operation cycle is performed after time of day t12. Moreover, the value of the block addresses A0-A1 at this time is "00", and shows that external access to 1st block 20A is demanded. Therefore, the external access implementation signal generating circuit 42 (drawing 5) sets external access implementation signal #EX0 (drawing 7 (k)) as L level (active), and on the other hand, the refresh implementation signal generating circuit 44 maintains refresh implementation signal #RF0 (drawing 7 (l)) on H level (inactive) for a while.
[0069] Since external access to block 20A is continuing at the time of day t13 of the next rising edge of clock signal ICLK, it is changeless on the level of external access implementation signal #EX0 and the refresh demand signal RFREQ0. On the other hand, at the time of day t14 of the following rising edge, block addresses A0-A1 are changing to the value which shows external access to 2nd block 20B further. So, in the cycle after time of day t14, external access implementation signal #EX0 to 1st block 20A is set to H level (inactive), and refresh implementation signal #RF0 is set to L level (active). Consequently, in the cycle after time of day t14, refresh actuation by 1st block 20A is performed. In addition, about refresh actuation of the whole chip, it mentions later further.
[0070] as mentioned above, in a standby cycle or an operation cycle, if what refresh actuation should be carried out for by refresh timing signal RFTM is notified, synchronizing with clock signal ICLK, the refresh (namely, external clock signal CLK -- synchronizing) demand signal RFREQ0 will occur, and refresh actuation will be started according to this.

[0071] drawing 8 -- a SUNUZU condition -- it is the timing chart which shows initiation of the refresh actuation to kick. Since the SUNUZU signal ZZ is maintained at L level in the state of SUNUZU, the output Q54 of NAND gate 54 is maintained at H level (drawing 8 (e)). Therefore, if refresh timing signal RFTM (drawing 8 (f)) starts in time of day t21 and the 1st latch's 56 output Q56 (drawing 8 (h)) also starts according to this, the output Q57 (drawing 8 (i)) of the AND gate 57 will start on H level. Moreover, the refresh demand signal RFREQ0 (drawing 8 (j)) which is the 2nd latch's 58 output also starts on H level according to this. Since external access is not performed in the state of SUNUZU, shortly after the refresh demand signal RFREQ0 is set to H level, refresh implementation signal #RF0 is surely set to L level (active), and refresh actuation is started. The actuation after this time is the same as that of drawing 6 .
[0072] Thus, shortly after what internal refresh should be performed for by refresh timing signal RFTM is notified in the state of SUNUZU, the refresh actuation in four blocks 20A-20D is started. Therefore, it is possible to perform refresh actuation only by the internal circuitry of a memory chip 200, without needing the external clock signal CLK and the internal clock signal ICLK in the state of SUNUZU.
[0073] Drawing 9 is a timing chart which shows the actuation in the case of shifting to an operation cycle from a SUNUZU condition. At the time of day t21 of drawing 9 , refresh actuation is started in the SUNUZU condition. Actuation (drawing 9 (e) - (m)) of each signal in case refresh is started is the same as drawing 8 .
[0074] If an operation cycle will be immediately started when refresh actuation is started in a SUNUZU condition (time of day t22 of drawing 9), refresh actuation and external access will collide in the first 1 cycle. Consequently, in the operation cycle which begins from time of day t22, it may be impossible to carry out external access (read-out and writing of data). For example, if a read cycle is performed from time of day t22, data cannot be read from the memory cell array 20, but the data in which the external device made a mistake from the I / O data terminals IO0-IO15 may be read.
[0075] Then, in the 1st example, when shifting to an operation cycle from a SUNUZU condition, the operation cycle is started, after performing a standby cycle once first, as shown in drawing 9 . If it carries out like this, also when refresh actuation is started just before termination of a SUNUZU condition, it is possible to perform right external access in an operation cycle (cycle after time of day t23).
[0076] In addition, as for an external device, it is common that it cannot recognize whether internal refresh is started just before termination of a SUNUZU condition. Therefore, after performing a standby cycle once first, it is always desirable, when shifting to an operation cycle from a SUNUZU condition to generate the input signal from an external device so that an operation cycle may be started.
[0077] In addition, 1 cycle first inserted in case it shifts to an operation cycle from a SUNUZU condition can be considered not only as a standby cycle but as the cycle (it is called "a non-operation cycle" below) of arbitration to

which external access is not performed. Moreover, such a non-operation cycle may be performed more than the two cycle that what is necessary is just to perform once [at least] in front of an operation cycle synchronizing with clock signal ICLK and CLK. However, it is more desirable for a non-operation cycle to consider only as 1 cycle from a viewpoint of processing speed.

[0078] Drawing 10 is the block diagram showing the internal configuration of line PURIDE coder 30A. Line PURIDE coder 30A is equipped with two switch & latch circuits 34 and 36 and judgment circuits 38. Other line PURIDE coders 30B-30D have the same configuration.

[0079] External access implementation signal #EX0 and refresh implementation signal #RF0 which were supplied to the judgment circuit 38 from block controller 40A are inputted. When external access implementation signal #EX0 is active (L level), the judgment circuit 38 sets up actively the latch signal LEX supplied to the 1st switch & latch circuit 34. The 1st switch & latch circuit 34 latches the line addresses A8-A19 inputted from the external device according to this latch signal LEX, and supplies them to line decoder 24A. At this time, the latch signal LRF supplied to the 2nd switch & circuit 36 is set up inactive, and the output from the 2nd switch & latch circuit 36 is forbidden.

[0080] On the other hand, when refresh implementation signal #RF0 is active (L level), the judgment circuit 38 sets up actively the latch signal LRF supplied to the 2nd switch & latch circuit 36. The 2nd switch & latch circuit 36 latches refresh addresses RFA8-RFA19 according to this latch signal LEX, and supplies them to line decoder 24A. At this time, the latch signal LEX supplied to the 1st switch & latch circuit 34 is set up inactive, and the output from the 1st switch & latch circuit 34 is forbidden.

[0081] In addition, block controller 40A (drawing 5) is constituted so that external access implementation signal #EX0 and refresh implementation signal #RF0 to the same block 20A may not be made active to coincidence. All, as for line PURIDE coder 30A, external access implementation signal #EX0 and refresh implementation signal #RF0 do not supply the address to line decoder 24A, when inactive.

[0082] Thus, line PURIDE coder 30A chooses and supplies one of the line addresses A8-A19 inputted from the external device, and the refresh addresses RFA8-RFA19 according to the level of external access implementation signal #EX0 and refresh implementation signal #RF0. Therefore, when external access is demanded from block 20A, according to line addresses A8-A19, one word line in block 20A is activated. On the other hand, when external access is not required from block 20A and refresh is demanded, according to refresh addresses RFA8-RFA19, refresh actuation about two or more memory cells on one word line of block 20A is performed.

[0083] Other blocks 20B-20D of the actuation of drawing 6 - drawing 9 mentioned above are the same. However, external access is performed only about one block specified by block addresses A0-A1, and external access is not performed to coincidence to two or more blocks. On the other hand, refresh actuation can be carried out to coincidence in four blocks 20A-20D so that it may explain below.

[0084] Refresh actuation of the whole A4. chip: Drawing 11 is a timing chart which shows refresh actuation of the whole chip in a standby cycle. If refresh timing signal RFTM (drawing 11 (e)) starts in time of day t1 as explained in drawing 6 , synchronizing with the next rising edge (time of day t2) of clock signal ICLK (drawing 11 (a)), the refresh demand signal RFREQ0 over block 20A will start on H level. At this time, the refresh demand signals RFREQ1-RFREQ3 over other blocks 20B-20D also start on H level at coincidence. In a standby cycle, since external access is not performed, external access request signal #EX0-#EX3 to four blocks 20A-20D is held at H level (inactive), and refresh implementation signal #RF 0-3 is set as L level (active). Consequently, in four blocks 20A-20D, all the memory cells on the n-th word line specified by the same refresh addresses RFA8-RFA19 (drawing 11 (t)) are refreshed. In addition, one refresh actuation is completed in 1 clock-period Tc (namely, cycle period of memory).

[0085] If all refresh actuation in four blocks 20A-20D is completed, four refresh demand signals RFREQ0-RFREQ3 (drawing 11 (f) - (i)) will return to L level. The refresh counter controller 90 (drawing 4) generates count-up signal #CNTUP (drawing 11 (s)) according to level change of these refresh demand signals RFREQ0-RFREQ3.

[0086] Drawing 12 is the block diagram showing the internal configuration of the refresh counter controller 90. This controller 90 is equipped with 4 input NOR gate 92, NAND gate 94, the delay circuit 96, and the inverter 98. Four refresh demand signals RFREQ0-RFREQ3 are inputted into 4 input NOR gate 92. The output Q92 of 4 input NOR gate 92 is inputted into one input terminal of NAND gate 94. Further, an output Q92 is delayed in a delay circuit 96, and after it is reversed with an inverter 98, it is inputted into the input terminal of another side of NAND gate 94. After four refresh demand signals RFREQ0-RFREQ3 fall to L level, both count-up signal #CNTUP(s) outputted from NAND gate 94 serve as a pulse signal from which only the time delay in a delay circuit 96 serves as L level, so that he can understand from this configuration (drawing 11 (s)).

[0087] The refresh counter 100 counts up one refresh addresses RFA8-RFA19 (drawing 11 (t)) according to this count-up signal #CNTUP. Therefore, the next refresh actuation is performed about the n+1st word lines.

[0088] Thus, in a standby cycle, since there is no external access also to the blocks [which] 20A-20D, refresh actuation is performed by coincidence in four blocks 20A-20D.
[0089] Drawing 13 is a timing chart which shows refresh actuation of the whole chip in an operation cycle. If refresh timing signal RFTM (drawing 13 (e)) starts in time of day t11 as explained also in drawing 7 , synchronizing with the next rising edge (time of day t12) of clock signal ICLK (drawing 13 (a)), the refresh demand signal RFREQ0 over block 20A will start on H level. At this time, the refresh demand signals RFREQ1-RFREQ3 over other blocks 20B-20D also start on H level at coincidence. The value of block addresses A0-A1 is "00", and this time of day t12 requires external access to the 1st block. Therefore, external access implementation signal #EX0 (drawing 13 (k)) to 1st block 20A is set as L level (active), and refresh implementation signal #RF0 is maintained by H level (inactive). The actuation so far is the same as what was explained to drawing 7 .
[0090] About other blocks 20B-20D with which external access is not demanded in time of day t12, external access implementation signal #EX1-#EX3 (drawing 13 (l) - (n)) is held at H level (inactive), and refresh implementation signal #RF0 (drawing 13 (p) - (r)) is set as L level (active). Therefore, in the cycle which begins from time of day t12, external access is performed to 1st block 20A, and refresh actuation is performed to other three blocks 20B-20D. The refresh demand signals RFREQ1-RFREQ3 about three blocks 20B-20D return to L level according to termination of refresh actuation. On the other hand, the refresh demand signal RFREQ0 over block 20A for which refresh actuation is suspended is maintained with H level.
[0091] In the rising edge (time of day t13) of the next clock signal ICLK, since external access to 1st block 20A is continued, refresh actuation in this block 20A is not performed. Therefore, the refresh demand signal RFREQ0 is maintained by H level.
[0092] Furthermore in the rising edge (time of day t14) of the next clock signal ICLK, block addresses A0-A1 are changing to the value which shows 2nd block 20B. Then, the external access implementation signal generating circuit 42 sets refresh implementation signal #RF0 (drawing 13 (o)) as L level (active), and performs refresh actuation while it starts external access implementation signal #EX0 (drawing 13 (k)) to 1st block 20A on H level (inactive). That is, in the starting cycle, refresh actuation is performed only in 1st block 20A from time of day t14. After this refresh actuation is completed, the refresh demand signal RFREQ0 returns to L level.
[0093] In this way, if all refresh actuation in four blocks 20A-20D is completed and four refresh demand signals RFREQ0-RFREQ3 return to L level, count-up signal #CNTUP (drawing 13 (s)) will occur, and one refresh addresses RFA8-RFA19 (drawing 13 (t)) will count up.
[0094] In addition, also when external access to the same block 20A is continuing more than 1 refresh period (period of refresh timing signal RFTM), it is considered. In such a case, before refresh addresses RFA8-RFA19 count up, the following refresh timing will arise. At this time, refresh about the n-th word line is again performed in the procedure of drawing 13 about four blocks 20A-20D. That is, in all blocks, since count-up of a refresh address is performed after the refresh actuation about the same refresh address is completed, it can perform certainly refresh about all the word lines of four blocks 20A-20D.
[0095] Thus, in an operation cycle, when refresh actuation is demanded, only the refresh actuation about the block with which external access is demanded is postponed, and refresh actuation is performed as it is in other three blocks. And termination of external access to the block with which external access was made performs refresh actuation to the block. There are some following advantages in such actuation.
[0096] The 1st advantage is a point that the permeability of refresh is securable. Here, when it regards as "permeability of refresh" from an external device, it means that external access is not overdue with internal refresh. That is, in an operation cycle, it is judged by each synchronizing with clock signal ICLK whether external access is performed with each block or refresh actuation is performed (to namely, external clock signal CLK). Moreover, refresh actuation is completed within 1 time of the cycle period Tc. Therefore, when there is a demand of external access, it can always perform immediately, without postponing the external access.
[0097] The 2nd advantage is a point which can perform refresh about all blocks, if the block set as the object of external access in the period is changing even if external access to a memory chip 200 carries out long duration continuation. The effect which raises the permeability of refresh further has this 2nd advantage. What is necessary is for there to be no necessity for 20 memory cell array of being divided into four blocks, and to just be divided into at least two blocks, in order to demonstrate such an advantage. However, as for the block set as the object of external access, changing as frequently as possible is desirable. What is necessary is for that just to assign 2 bits which changes as frequently as possible as block addresses A0-A1. Usually, it is in the orientation for a lower-ranking bit to tend to change, in two or more address bits. Therefore, it is desirable to assign several least significant bits in two or more address bits as a block address for generally identifying two or more blocks of a memory cell array.

[0098] Drawing 14 is a timing chart which shows refresh actuation of the whole chip in a SUNUZU condition. As drawing 8 also explained, shortly after refresh timing signal RFTM (drawing 14 (e)) starts in time of day t21, the refresh demand signals RFREQ0-RFREQ3 over four blocks 20A-20D start on H level. Since external access is not performed in the state of SUNUZU, external access implementation signal #EX0-#EX3 to four blocks 20A-20D is maintained by H level (inactive), and refresh implementation signal #RF0 - #RF3 fall to L level (active). Consequently, in four blocks 20A-20D, all the memory cells on the n-th same word line are refreshed. Subsequent actuation is the same as the thing of the standby cycle shown in drawing 11 .
[0099] Thus, in the SUNUZU condition, shortly after the initiation timing of refresh actuation does not synchronize with clock signal ICLK but the initiation stage of refresh actuation is shown by refresh timing signal RFTM, refresh actuation is performed by coincidence in four blocks 20A-20D.
[0100] As explained above, since the memory chip 200 of the 1st example has judged the demand of external access, and the demand of internal refresh to coincidence synchronizing with a clock signal CLK, it does not delay external access in an operation cycle. Moreover, since refresh is performed to all blocks 20A-20D when refresh is required by refresh timing signal RFTM in the state of SUNUZU, it is possible to refresh, even if clock signal ICLK is not supplied from an external device.
[0101] That is, since the signal (clock signal ICLK and refresh timing signal RFTM) which determines the initiation timing of refresh actuation in an operation cycle and a SUNUZU condition is changed in the 1st example, it is possible to perform refresh actuation suitable for each condition. In an operation cycle, refresh actuation can be performed so that the permeability of refresh may be held, and specifically, it is possible to perform refresh actuation certainly on the other hand in the operating state of the low power which does not use clock signal ICLK in the state of SUNUZU.
[0102] Moreover, even if internal refresh is started just before shifting to an operation cycle since one cycle of standby cycles is inserted before an operation cycle in case it shifts to an operation cycle from a SUNUZU condition, internal refresh is completed by the operation cycle, therefore the collision with internal refresh and external access is avoided.
[0103] B. The 2nd example : drawing 15 is explanatory drawing showing the configuration of the terminal of the memory chip 300 as the 2nd example of this invention. This memory chip 300 does not have the clock input terminal CLK, but has the feature that no necessity of inputting the external clock signal CLK is. An external device (for example, CPU) can access this memory chip 300 in the same procedure as the usual asynchronous type SRAM.
[0104] Moreover, the address transition detector (it is hereafter called a "ATD circuit") 110 for detecting that any 1 bits or more in input/output addresses A0-A19 changed is established in the interior of this memory chip 300. The ATD signal generated by the ATD circuit 110 has the almost same work as clock signal ICLK in the 1st example so that it may mention later.
[0105] Drawing 16 is explanatory drawing showing the partition of the operating state of the memory chip 300 of the 2nd example. The difference from the 1st example (drawing 2) is only the point that the ATD signal is used instead of clock signal ICLK, in the 1st refresh mode 1. That is, in the 1st refresh mode, after the refresh timer 70 generates a refresh timing signal, refresh is started synchronizing with an ATD signal. In the 2nd refresh mode, like the 1st example, shortly after the refresh timer 70 generates a refresh timing signal, refresh actuation is started.
[0106] Drawing 17 is a timing chart which shows the outline of actuation of the memory chip 200 of the 2nd example. Also in the 2nd example, three operating state (operation, standby, SUNUZU) is the same as the 1st example shown in drawing 3 almost. However, in the 2nd example, it differs from the 1st example in that input/output addresses A0-A19 do not change in principle except an operation cycle. Therefore, it is judged at any time according to change of chip select signal #CS and the SUNUZU signal ZZ any of three operating state (operation, standby, SUNUZU) they are.
[0107] In addition, cycle period Tc' (namely, the shortest period of change of the addresses A0-A19) of the operation cycle in the memory chip 300 of the 2nd example is longer than the cycle period Tc of the memory chip 200 of the 1st example a little. About this reason, it mentions later.
[0108] Drawing 18 is the block diagram showing the internal configuration of the memory chip 300 of the 2nd example. The difference from the 1st example shown in drawing 4 is the point that the ATD circuit 110 is formed instead of the clock controller 80, and others are the same as the 1st example. An ATD signal is generated, when it detects whether the ATD circuit 110 has change in any 1 bits or more in the input/output addresses A0-A19 supplied from the external device and change is detected.
[0109] Drawing 19 is the block diagram showing the internal configuration of the ATD circuit 110. The ATD circuit 110 is equipped with 20 transition detectors 111 corresponding to each bit of the 20-bit input/output addresses A0-A19, and 20 input OR gates 118. Each transition detector 111 has an inverter 112, two pulse generating circuits 113,114, and OR gates 115. As a pulse generating circuit 113,114, a one-shot multivibrator is used, for example.
[0110] The 1st pulse generating circuit 113 generates one pulse which has predetermined pulse width according to the

rising edge of the address bit A0. Moreover, an inverter 112 and the 2nd pulse generating circuit 114 generate one pulse which has predetermined pulse width according to the falling edge of the address bit A0. Therefore, from the OR gate 115, one pulse is outputted at a time for every edge of the rising edge of the address bit A0, and a falling edge. This is the same about other address bits A1-A19.

[0111] The output of 20 transition detectors 111 is inputted into 20 input OR gate 118. Therefore, change of the level of one or more bits in the 20-bit input/output addresses A0-A19 outputs a pulse-like ATD signal from the OR gate 118. As shown in drawing 18 , this ATD signal is supplied to an address buffer 60 or the refresh demand signal generating circuits 50A-50D, and performs the same work as clock signal ICLK in the 1st example.

[0112] Drawing 20 is the block diagram showing the internal configuration of refresh demand signal generating circuit 50A in the 2nd example, and block controller 40A. The difference from drawing 5 explained in the 1st example is only the point that clock signal ICLK is transposed to the ATD signal, and others are the same as the 1st example.

[0113] Drawing 21 is a timing chart which shows initiation of the refresh actuation in the standby cycle of the 2nd example. In the memory chip 300 of the 2nd example, input/output addresses A0-A19 do not change in principle in a standby cycle. However, as drawing 16 explained, in the standby cycle, the 1st refresh mode which performs refresh synchronizing with an ATD signal is adopted. Then, an external device changes periodically at least one address bit (for example, A0) during the period of a standby cycle, and performs internal refresh. As for the period of such change of an address bit, it is desirable that it is 1/2 or less [of the refresh period specified by refresh timing signal RFTM]. If an address bit changes for every 1/2 or less period of a refresh period, refresh timing signal RFTM of this reason will be because an ATD signal surely occurs in the period of H level.

[0114] In the time of day t1 of drawing 21 , refresh timing signal RFTM (drawing 21 (g)) starts on H level, and an ATD signal occurs according to change of the addresses A0-A19 (drawing 21 (d)) in time of day t2 (drawing 21 (a)). Next actuation is the same as actuation of the 1st example explained by drawing 6 .

[0115] Drawing 22 is a timing chart which shows initiation of the refresh actuation in the operation cycle of the 2nd example. In an operation cycle, since the addresses A0-A19 change to every 1 cycle period Tc', refresh actuation becomes the same thing as actuation of the 1st example shown in drawing 7 .

[0116] drawing 23 -- the SUNUZU condition of the 2nd example -- it is the timing chart which shows initiation of the refresh actuation to kick. Refresh actuation is started shortly after the timing of refresh is notified by refresh timing signal RFTM in a SUNUZU condition like the 1st example also in the 2nd example. Therefore, it is possible to perform refresh actuation only by the internal circuitry of a memory chip 200, without needing change of the addresses A0-A19 inputted from an external device in the state of SUNUZU.

[0117] In the 2nd example, the addresses A0-A19 are equivalent to "the external timing signal used with a refresh timing signal in case the activation timing of refresh actuation is determined" in this invention so that he can understand from above-mentioned explanation.

[0118] Drawing 24 is a timing chart which shows the case where it shifts to an operation cycle from a SUNUZU condition in the 2nd example. At time of day t21, refresh actuation is started in the SUNUZU condition. Actuation (drawing 24 (e) - (m)) of each signal in case refresh is started is the same as drawing 23 . At time of day t22, refresh implementation signal #RF0 (drawing 24 (l)) is set as L level (active), and the refresh in 1st block 20A is started according to this.

[0119] In the example of drawing 24 , in this time of day t22, chip select signal #CS and the SUNUZU signal ZZ change, and the operation cycle is started. Since refresh is already started at this time, external access is performed after this refresh is completed. That is, only time amount Td is from the time of day t22 when the operation cycle started in external access implementation signal #EX0 (drawing 24 (k)), and it is set to L level (active).

[0120] Case [like drawing 24], the timing of external access implementation signal #EX0 in an operation cycle is set up so that it can always suit. That is, in an operation cycle, from the time of day (time of day when chip select signal #CS specifically changes from H level to L level) when an operation cycle is started, the level of external access implementation signal #EX0 is set up so that only the predetermined time delay Td may be overdue and external access may be started. As for this, the same is said of external access implementation signal #EX1-#EX3 to other blocks.

[0121] cycle period Tc' of the memory chip 300 of the 2nd example -- a case like drawing 24 -- also setting -- external access -- cycle period [1 time of] Tc' -- it is desirable to be set up sufficiently long so that it may end inside. That is, even if the length of cycle period Tc' assumes the case where internal refresh is exactly started in the time of day when an operation cycle is started, it is desirable to be set up so that external access can be completed in the operation cycle. Since external access can be completed in cycle [1 time of] period Tc' even case [like drawing 24] if it does in this way, an external device can access a memory chip 300 to the timing of arbitration, without taking internal refresh into consideration. It is possible to raise the permeability of refresh by this.

[0122] In addition, in the 1st example mentioned above, as drawing 9 explained, when shifting to an operation cycle from a SUNUZU condition, the collision with internal refresh and external access was avoided by inserting the standby cycle for 1 cycle. The reason in which such actuation is possible is that the operation cycle and the standby cycle are performed synchronizing with the external clock signal CLK.
[0123] On the other hand, in the 2nd example, since the external clock signal CLK is not used, it is not necessarily easy to insert a standby cycle like drawing 9 . So, in the 2nd example, the collision with the internal refresh and external access in the worst case is avoided by setting up cycle period Tc' comparatively long.
[0124] Thus, since cycle period Tc' in the memory chip 300 of the 2nd example is longer than the cycle period Tc in the memory chip 200 of the 1st example, from the point of a speed of operation, its memory chip 200 of the 1st example is more desirable. On the other hand, the memory chip 300 of the 2nd example has the advantage with the unnecessary and input of the external clock signal CLK of being easy to use rather than the memory chip 200 of the 1st example since it is the same as asynchronous [usual in the procedure of access of an external device / SRAM].
[0125] In addition, since refresh actuation of the whole chip in the 2nd example is almost the same as the 1st example mentioned above, explanation is omitted.
[0126] As mentioned above, in the memory chip 200,300 of the 1st and 2nd examples, internal refresh is performed in the 1st refresh mode according to the timing determined by the clock signal CLK or the addresses A0-A19 which are supplied from an external device after generating of refresh timing signal RFTM. Moreover, in the 2nd refresh mode, internal refresh is immediately performed according to generating of refresh timing signal RFTM. That is, it is possible to perform internal refresh in the mode which was suitable for the operating state of a memory chip 200,300, respectively.
[0127] C. The example of application to electronic equipment : drawing 25 is the perspective diagram using the semiconductor memory equipment by this invention of the portable telephone as one example of electronic equipment. This portable telephone 600 is equipped with the main part section 610 and a covering device 620. A keyboard 612, the liquid crystal display section 614, the receiver section 616, and the main part antenna section 618 are formed in the main part section 610. Moreover, the transmission section 622 is formed in the covering device 620.
[0128] Drawing 26 is the block diagram showing the electric configuration of a portable telephone 600. A keyboard 612, the LCD driver 632 for driving the liquid crystal display section 614, SRAM640, and VSRAM642 and EEPROM644 are connected to CPU630 through the bus line which is not illustrated.
[0129] SRAM640 is used, for example as high-speed cache memory. Moreover, VRAM642 is used as activity memory for image processings. As this VSRAM642 (called false [SRAM] or Imagination SRAM), the memory chip 200 of the 1st example mentioned above and the memory chip 300 of the 2nd example are employable. Since various kinds of set points of a portable telephone 600 are stored, EEPROM644 is used.
[0130] When stopping actuation of a portable telephone 600 temporarily, VSRAM642 can be maintained in the SUNUZU condition. If it carries out like this, since VSRAM642 will perform internal refresh automatically, it is possible to hold without vanishing the data in VSRAM642. Since especially the memory chip 200,300 of each example mentioned above is large capacity comparatively, it has the advantage that holding a lot of data, such as image data, can be continued for a long time.
[0131] D. Modification : in addition, this invention can be carried out in various modes in the range which is not restricted to an above-mentioned example or an above-mentioned operation gestalt, and does not deviate from that summary, for example, the following deformation is also possible for it.
[0132] D1. modification 1: In the above-mentioned example, although refresh actuation was performed according to the 1st refresh mode in the standby cycle, in a standby cycle, it may be made to perform refresh actuation according to the 2nd refresh mode. Moreover, according to other different refresh modes from the 1st and 2nd refresh mode, it may be made to perform refresh actuation.
[0133] D2. modification 2: In the 1st refresh mode, by the 1st example of the above, synchronizing with the external clock signal CLK, refresh actuation was started after rising edge generating of refresh timing signal RFTM, and, on the other hand, refresh actuation was started after generating of refresh timing signal RFTM in the 2nd example synchronizing with the ATD signal (namely, change of the addresses A0-A19). However, as a signal (it is called a "external timing signal") for determining the timing which starts refresh actuation in the 1st refresh mode, it is also possible to use the external clock signal CLK and signals other than address A0 - A19. That is, what is necessary is just to start refresh actuation according to the timing generally determined in the 1st refresh mode by the external timing signal supplied from an external device.
[0134] D3. modification 3: After refresh timing signal RFTM instead occurs and predetermined carries out period progress further, you may make it start refresh actuation in the 2nd refresh mode, in each above-mentioned example,

although refresh actuation was immediately started after generating of refresh timing signal RFTM. Namely, what is necessary is making it just make a memory cell array start refresh actuation irrespective of the existence of an external timing signal in the 2nd refresh mode generally according to generating of refresh timing signal RFTM.

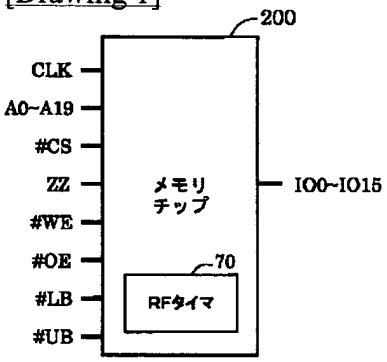
[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]

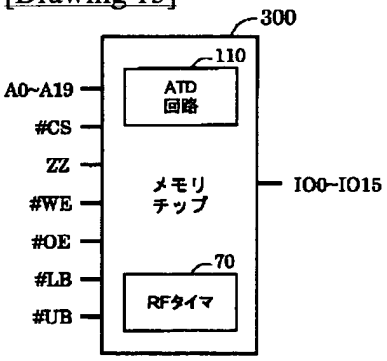


[Drawing 2]

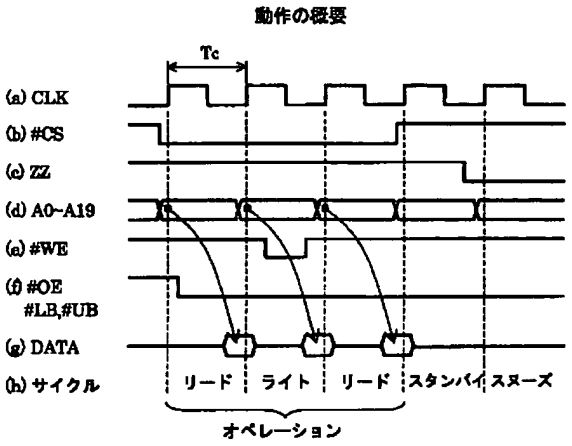
	#CS	ZZ	リフレッシュモード（注）
オペレーション	L	H	モード1
スタンバイ	H	H	モード1
スヌーズ（パワーダウン）	H	L	モード2

（注）
リフレッシュモード1：メモリチップ内部でリフレッシュタイミング信号が発生した後に、クロック信号CLKに同期してリフレッシュを実行する
リフレッシュモード2：メモリチップ内部でのリフレッシュタイミング信号の発生に応じてリフレッシュを実行する（クロック信号CLKは不要）

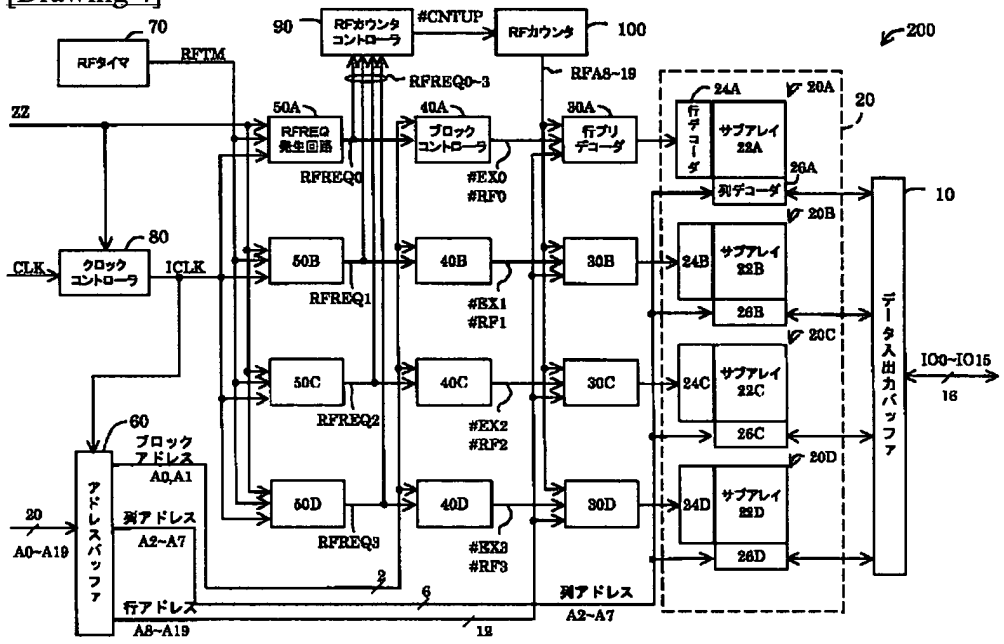
[Drawing 15]



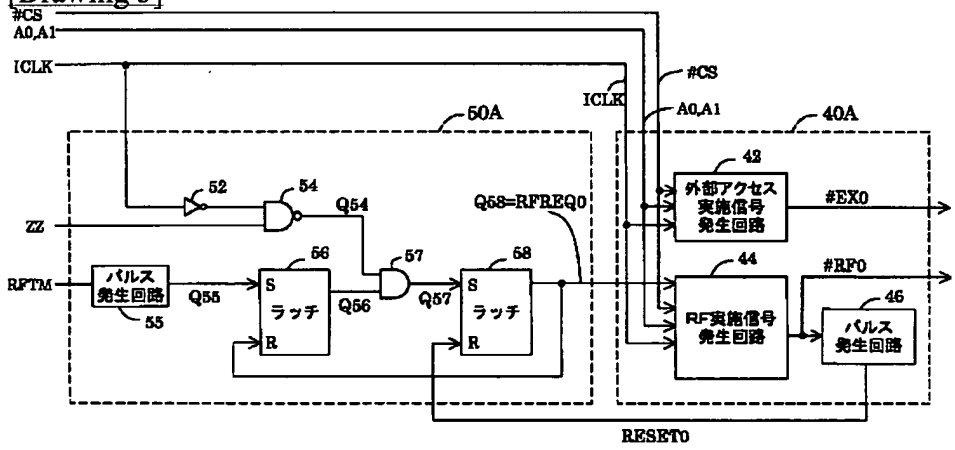
[Drawing 3]



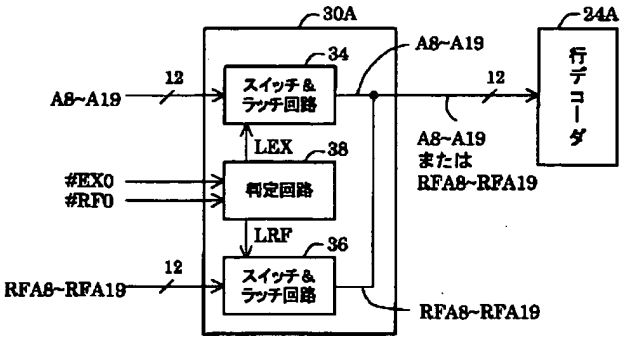
[Drawing 4]



[Drawing 5]

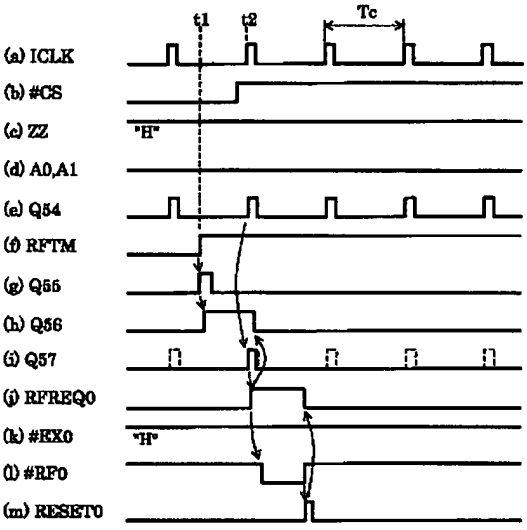


[Drawing 10]



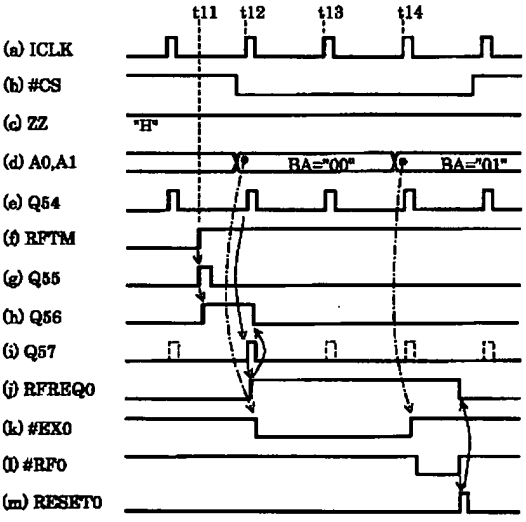
[Drawing 6]

スタンバイサイクルでのリフレッシュ動作の開始

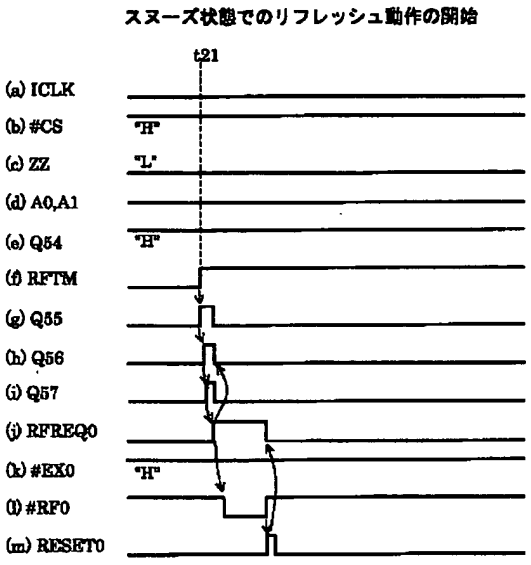


[Drawing 7]

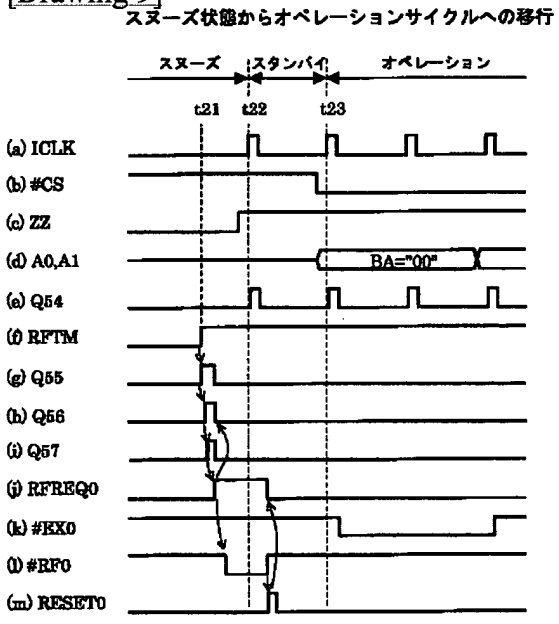
オペレーションサイクルでのリフレッシュ動作の開始



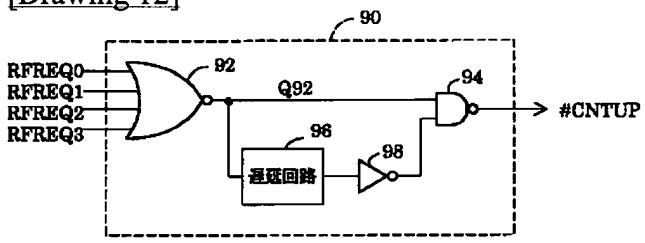
[Drawing 8]



[Drawing 9]

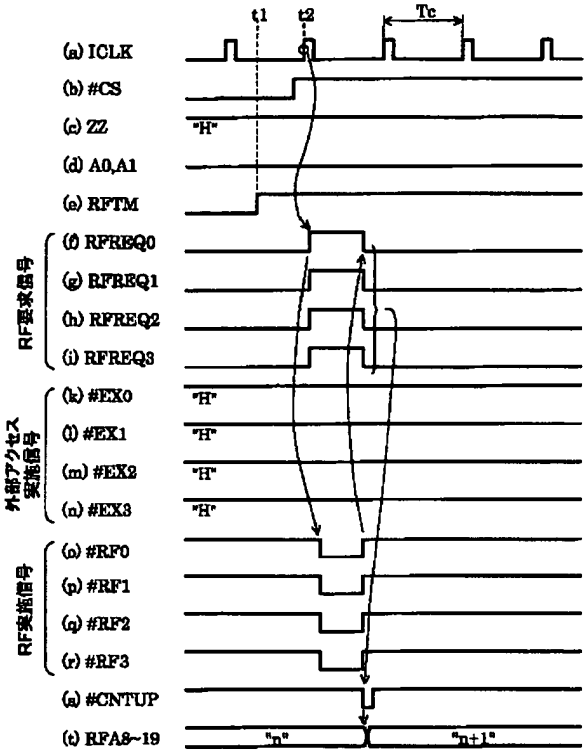


[Drawing 12]



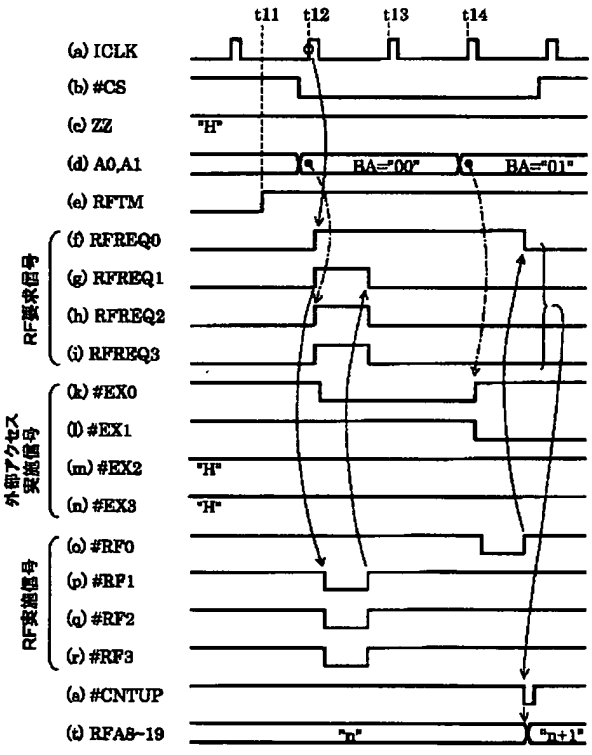
[Drawing 11]

スタンバイサイクルでのチップ全体のリフレッシュ動作



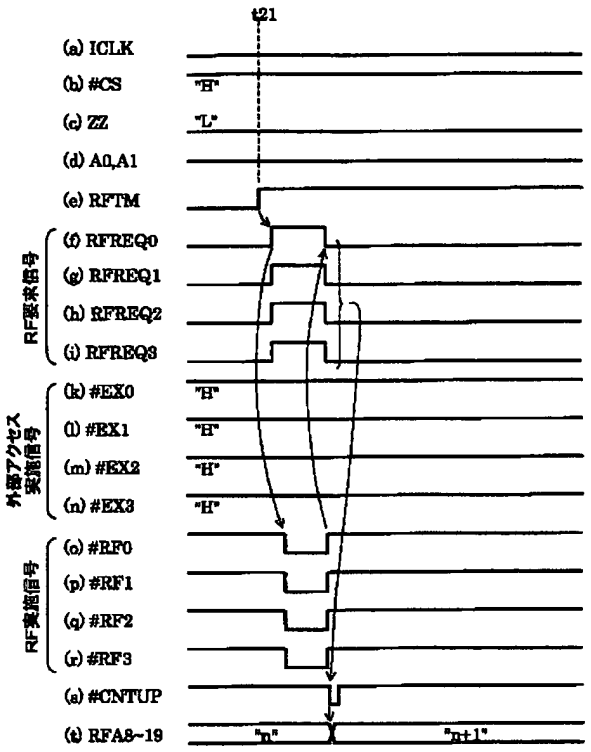
[Drawing 13]

オペレーションサイクルでのチップ全体のリフレッシュ動作



[Drawing 14]

スヌーズ状態でのチップ全体のリフレッシュ動作



[Drawing 16]

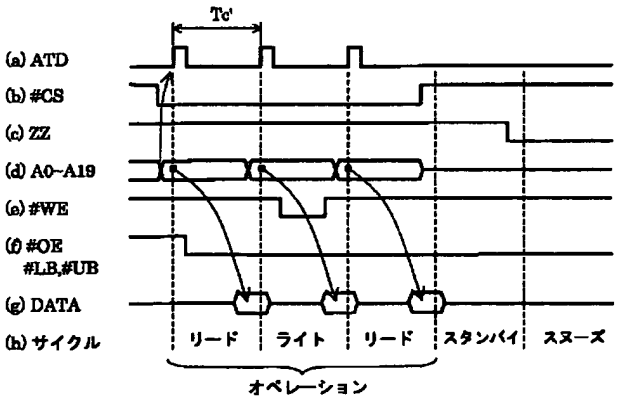
	#CS	ZZ	リフレッシュモード（注）
オペレーション	L	H	モード1
スタンバイ	H	H	モード1
スヌーズ（パワーダウン）	H	L	モード2

（注）
リフレッシュモード1： メモリチップ内部でリフレッシュタイミング信号が発生した後に、ATD信号に同期してリフレッシュを実行する

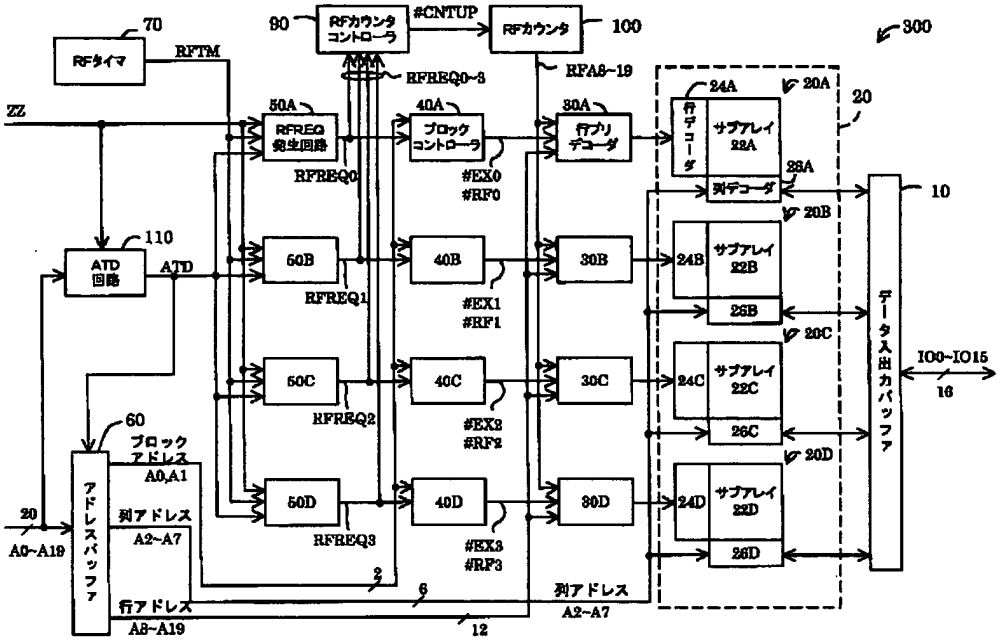
リフレッシュモード2： メモリチップ内部でのリフレッシュタイミング信号の発生に応じてリフレッシュを実行する（アドレス入力は不要）

[Drawing 17]

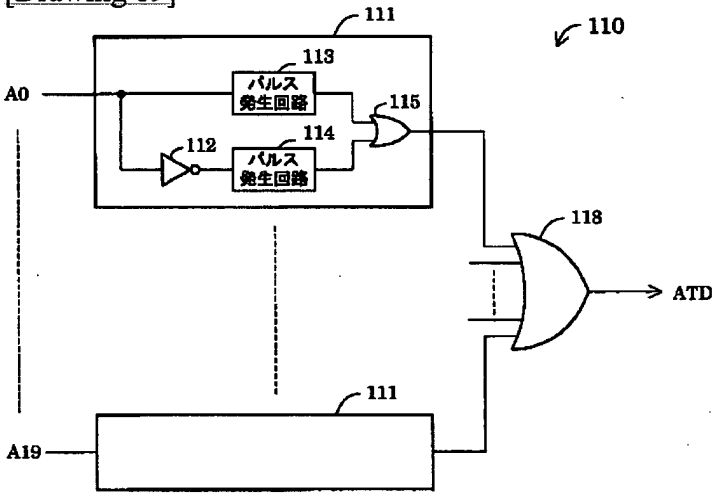
動作の概要



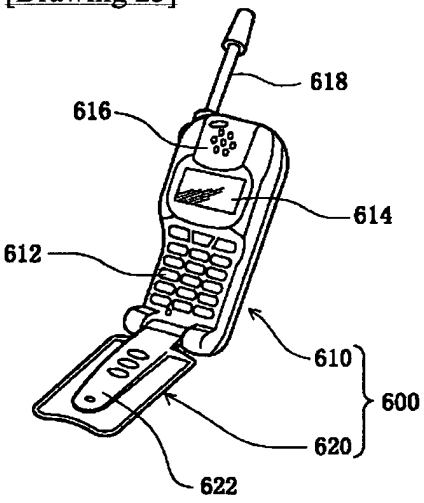
[Drawing 18]



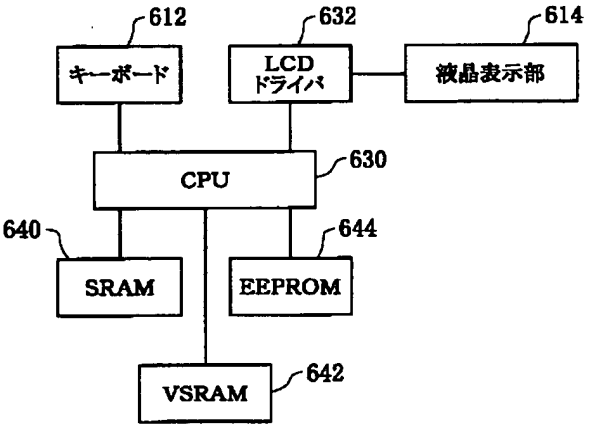
[Drawing 19]



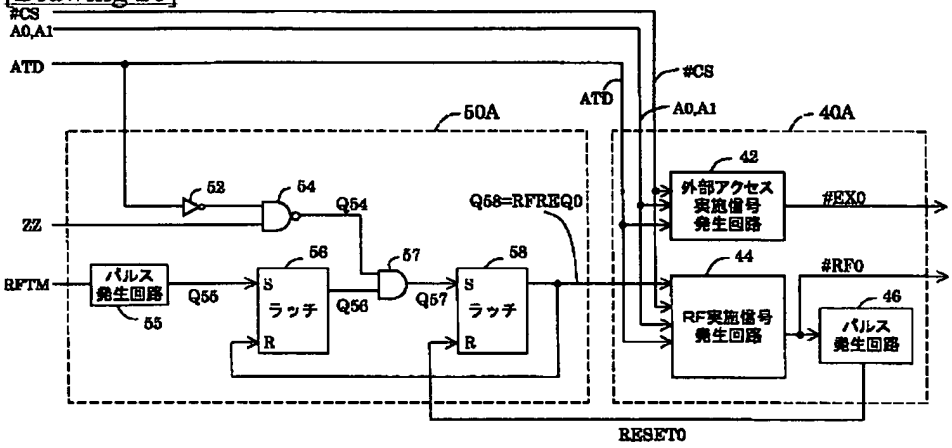
[Drawing 25]



[Drawing 26]

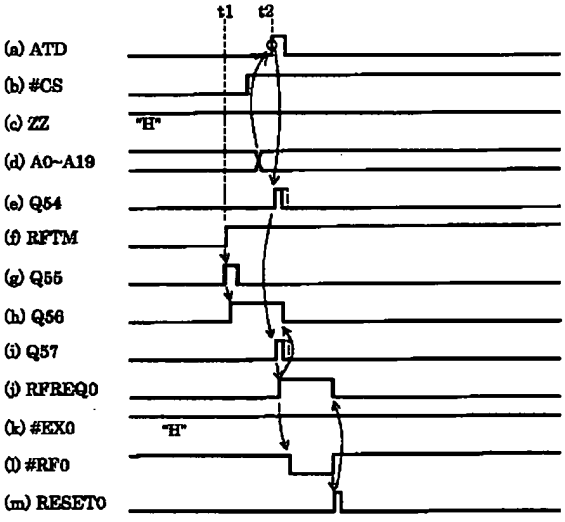


[Drawing 20]



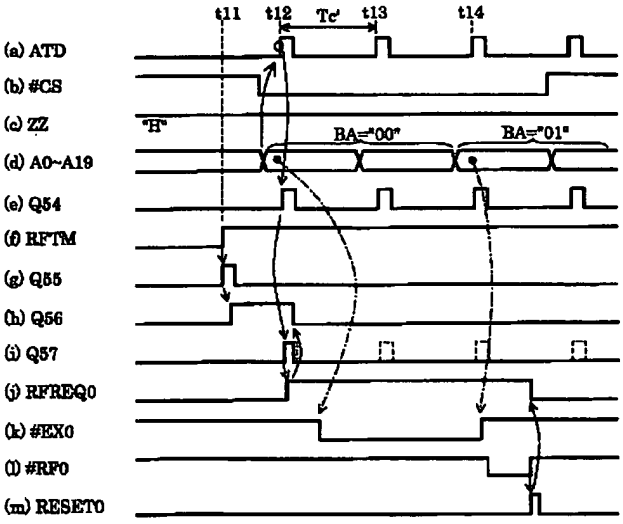
[Drawing 21]

スタンバイサイクルでのリフレッシュ動作の開始



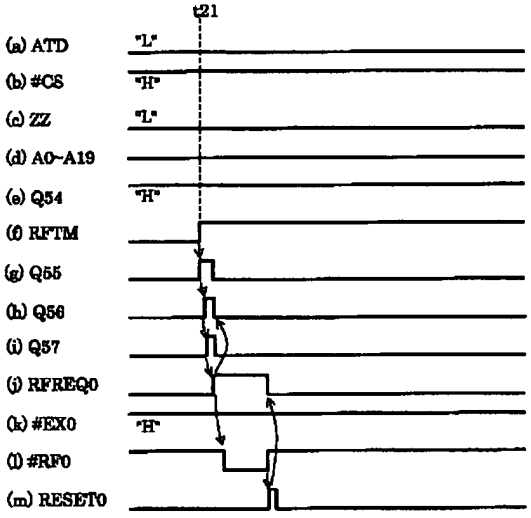
[Drawing 22]

オペレーションサイクルでのリフレッシュ動作の開始



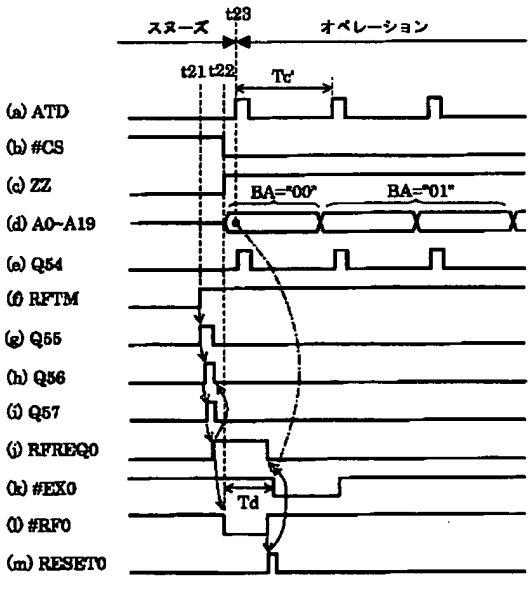
[Drawing 23]

スヌーズ状態でのリフレッシュ動作の開始



[Drawing 24]

スヌーズ状態からオペレーションサイクルへの移行



[Translation done.]